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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,697	09/30/2004	Ronald G. Filippi	FIS920040188US1	5696

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EXAMINER
AU, BAC H

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PTOCommunications@hwdpatents.com
efiplaw@us.ibm.com

Office Action Summary	Application No.	Applicant(s)	
	10/711,697	FILIPPI ET AL.	
	Examiner	Art Unit	
	Bac H. Au	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-8,11 and 13-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-8,11 and 13-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on April 1, 2008, in which claims 1, 11, and 17 were amended, and claims 9-10 were cancelled, has been entered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nitta (U.S. Pub. 2001/0054764) in view of Dubin (U.S. Pat. 6359328) and Roberts (U.S. Pat. 6204143).

Regarding claims 1 and 7, Nitta [Figs.6A-D] discloses a method of forming a gas dielectric structure for a semiconductor structure, the method comprising the steps of:

forming an opening [13] for semiconductor structure in a dielectric layer [12] on a substrate [11], wherein the opening includes a wiring opening;

depositing a sacrificial layer [41] over the opening such that the sacrificial layer fails to substantially fill the opening;

performing a directional etch on the sacrificial layer to form a sacrificial layer sidewall [41] on the opening after depositing the sacrificial layer; wherein the directional

etching removes the sacrificial layer only from substantially horizontal surfaces [Para.74];

depositing a conductive liner [14] over the opening after performing the directional etch;

depositing a metal [16] in the opening after depositing the conductive liner to form a wire;

planarizing the metal and the conductive liner [Fig.6C] after depositing the metal;

removing the sacrificial layer sidewall after the metal and the conductive liner are planarized, forming a void [15a], wherein the void extends along a side of the contact wire; and

depositing a cap layer [17] over the void to form the gas dielectric structure;

wherein the conductive liner includes at least one of the group consisting of: tantalum (Ta), tantalum nitride (TaN), titanium (Ti), titanium nitride (TiN), tungsten (W) and niobium (Nb) [Para.75].

Nitta [Paras.1-7] discloses a multilevel wiring layer can be formed, using the damascene process described. Nitta fails to explicitly disclose

wherein the opening includes both a wiring opening and a via opening,

wherein the via provides a vertical connection to an interconnect line;

depositing a metal to form a contact via; and

wherein the void extends along a side of the contact via.

However, it would be obvious that the process described in Nitta [Paras.1-7] would include forming both a wiring opening and a via opening to provide vertical interconnection between the levels. To better teach a via opening and forming a contact via as claimed, Dubin is hereby discussed.

Dubin [Figs.1-5] discloses a method of forming a gas dielectric structure for a semiconductor structure

wherein the opening includes both a wiring opening [18c] and a via opening [18a,b],

wherein the via [22a,b] provides a vertical connection to an interconnect line;

depositing a metal to form a contact via [Fig.2]; and

wherein the void [24a,b] extends along a side of the contact via.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Dubin into the method of Nitta to include the limitations above. The ordinary artisan would have been motivated to modify Nitta in the manner set forth above for at least the purpose of having an improved method of making high aspect ratio contact plugs and wiring [Dubin; col.2 lines 13-17].

Nitta [Para.76] discloses removing the sacrificial layer using a wet etching process, but fails to disclose using a dry etching process. However, Roberts [Figs.2-3; col.3 lines 18-19] discloses a method comprising removing a sacrificial layer using a dry etching process. Roberts makes obvious the suitable alternatives of wet and dry

etching processes in removing a sacrificial layer. It would have been obvious to one of ordinary skill in the art to utilize a dry etching process, as one of ordinary skill has good reason to pursue the known options within his or her technical grasp, to achieve the desired etching selectivity based on the structure and the material being used.

3. Claims 4-5, 11, 13, 15, 17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nitta (U.S. Pub. 2001/0054764) in view of Dubin (U.S. Pat. 6359328), Roberts (U.S. Pat. 6204143), and Cooney (U.S. Pub. 2004/0018714).

Regarding claims 4-5, 11, 13, and 17, Nitta, Dubin, and Roberts disclose most of the limitations of the claims as discussed above in the treatment of claim 1, wherein the wiring layer is formed by a damascene process, but fails to explicitly disclose

performing a dual damascene process; a via-first dual damascene process; to form an opening including a wiring opening and a via opening in a dielectric layer on a substrate;

wherein the forming step includes depositing a hard mask, patterning the hard mask and etching the hard mask.

However, Cooney [Figs.13-26] discloses

performing a dual damascene process; a via-first dual damascene process; to form an opening including a wiring opening and a via opening in a dielectric layer on a substrate;

wherein the forming step includes depositing a hard mask [106], patterning the hard mask and etching the hard mask.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Cooney into the method of Nitta, Dubin, and Roberts to include performing a dual damascene process; a via-first dual damascene process; to form an opening including at least one wiring opening and at least one via in a dielectric layer on a substrate; and wherein the forming step includes depositing a hard mask, patterning the hard mask and etching the hard mask. The ordinary artisan would have been motivated to modify Nitta, Dubin, and Roberts in the manner set forth above for at least the purpose of having a mask layer which would provide additional process flexibility in the formation of openings in the dielectric layer. Using hard masks and performing dual and via-first damascene processes are well-known in the art and are general knowledge to the ordinary artisan.

Regarding claims 15, and 19, Nitta discloses these limitations as discussed above in claim 7.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nitta (U.S. Pub. 2001/0054764) in view of Dubin (U.S. Pat. 6359328) and Roberts (U.S. Pat. 6204143), as applied to claim 1 above, and further in view of Parekh (U.S. Pat. 6214727).

Regarding claim 8, Nitta discloses the sacrificial layer [41] comprises silicon nitride (SiN), but fails to explicitly disclose wherein the sacrificial layer includes one of the group consisting of: aluminum (Al), and silicon dioxide. However, Parekh [Figs.9-

13] discloses a method wherein the sacrificial layer [104] includes one of the group consisting of: aluminum (Al), and silicon dioxide [Col.5 lines 48-59]. Parekh discloses and makes it obvious that the sacrificial layer can be either silicon nitride or silicon oxide. It would have been obvious to one skilled in the art to substitute one method for the other to achieve the predictable result of having a sacrificial layer that was selectively etchable relative to adjacent layers.

Claims 16 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nitta (U.S. Pub. 2001/0054764) in view of Dubin (U.S. Pat. 6359328), Roberts (U.S. Pat. 6204143), and Cooney (U.S. Pub. 2004/0018714), as applied to claims 11 and 17 above, and further in view of Parekh (U.S. Pat. 6214727).

Regarding claims 16 and 20, the limitations were discussed above in claim 8.

5. Claims 6, 11, 14, 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nitta (U.S. Pub. 2001/0054764) in view of Dubin (U.S. Pat. 6359328), Roberts (U.S. Pat. 6204143), and Tsai (U.S. Pub. 2003/0077897).

Regarding claims 6, 11, 14, 17 and 18, Nitta, Dubin, and Roberts disclose most of the limitations of the claims as discussed above, wherein the wiring layer is formed by a damascene process, but fails to explicitly disclose

performing a dual damascene process; a via-first dual damascene process; to form an opening including a wiring opening and a via opening in a dielectric layer on a substrate; and

further comprising the step of depositing a non-conductive liner prior to the step of depositing the sacrificial layer, wherein the non-conductive liner includes one of the group consisting of: silicon nitride (Si_3N_4) and silicon dioxide (SiO_2).

However, Tsai [Figs.1a-f, 2c] discloses the method comprising the step of performing a dual damascene process; a via-first dual damascene process; to form an opening including a wiring opening and a via opening in a dielectric layer on a substrate; and depositing a non-conductive liner [250] prior to the step of depositing the sacrificial layer, wherein the non-conductive liner includes one of the group consisting of: silicon nitride (Si_3N_4) and silicon dioxide (SiO_2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Tsai into the method of Nitta, Dubin, and Roberts to include in the method further comprising the step of depositing a non-conductive liner prior to the step of depositing the sacrificial layer, wherein the non-conductive liner includes one of the group consisting of: silicon nitride (Si_3N_4) and silicon dioxide (SiO_2). The ordinary artisan would have been motivated to modify Nitta, Dubin, and Roberts in the manner set forth above for at least the purpose of forming a protective layer to prevent via poisoning in subsequent processing steps [Tsai; para.17].

Response to Arguments

6. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection. The Action is made Final.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bac H. Au whose telephone number is 571-272-8795. The examiner can normally be reached on Mon-Fri 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Zandra V. Smith/
Supervisory Patent Examiner, Art Unit 2822

/B. H. A./
Examiner, Art Unit 2822